Noise Sources in Switched-Capacitor Delta-Sigma Modulators

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Outline For This Presentation

Noise Source in SC Delta-Sigma Modulators

☞ General Overview of Noise Sources in Delta-Sigma Modulators

Thermal Noise

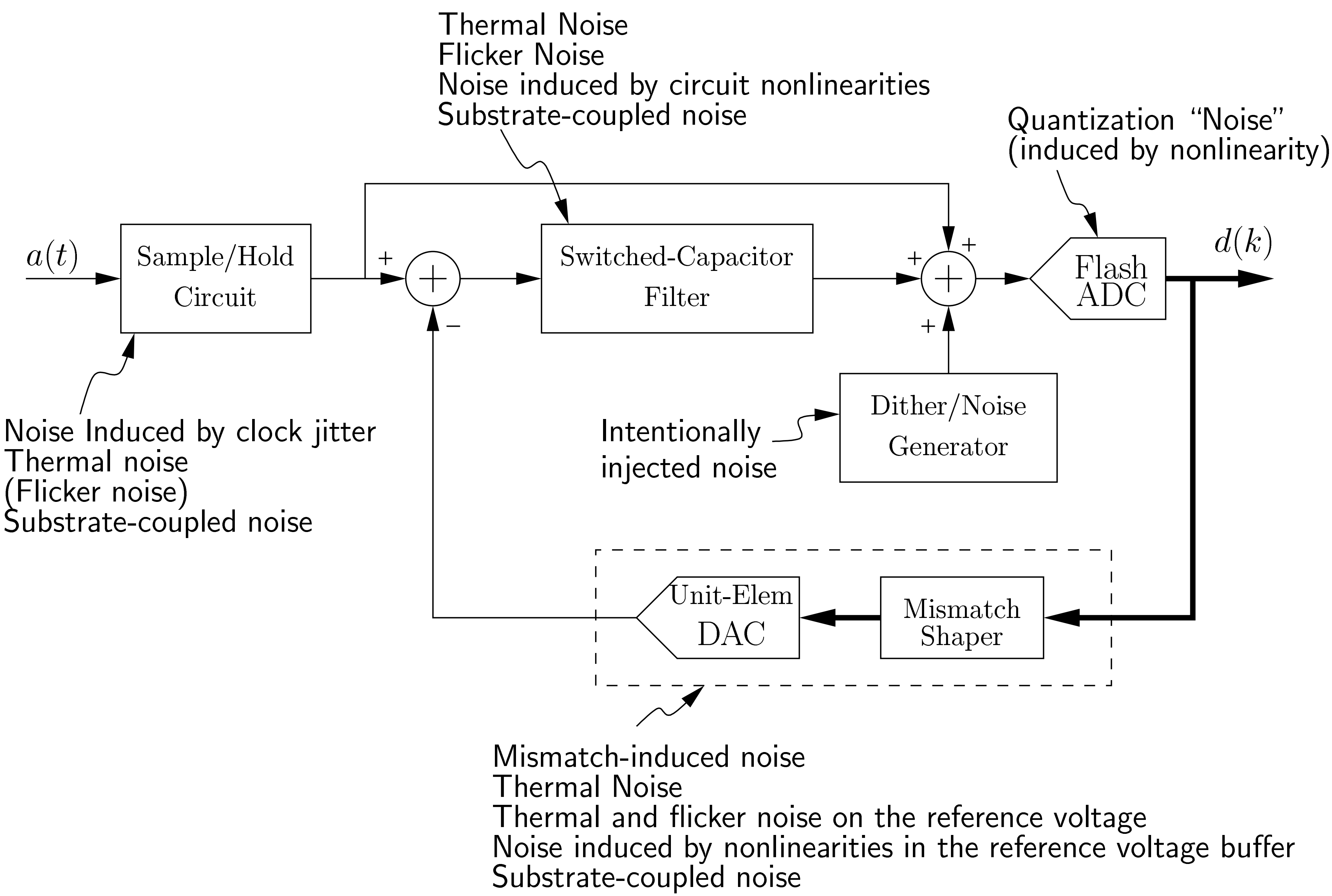
Flicker Noise (CDS, Chopper Techniques)

Clock Jitter Induced Noise (DT and CT Systems)

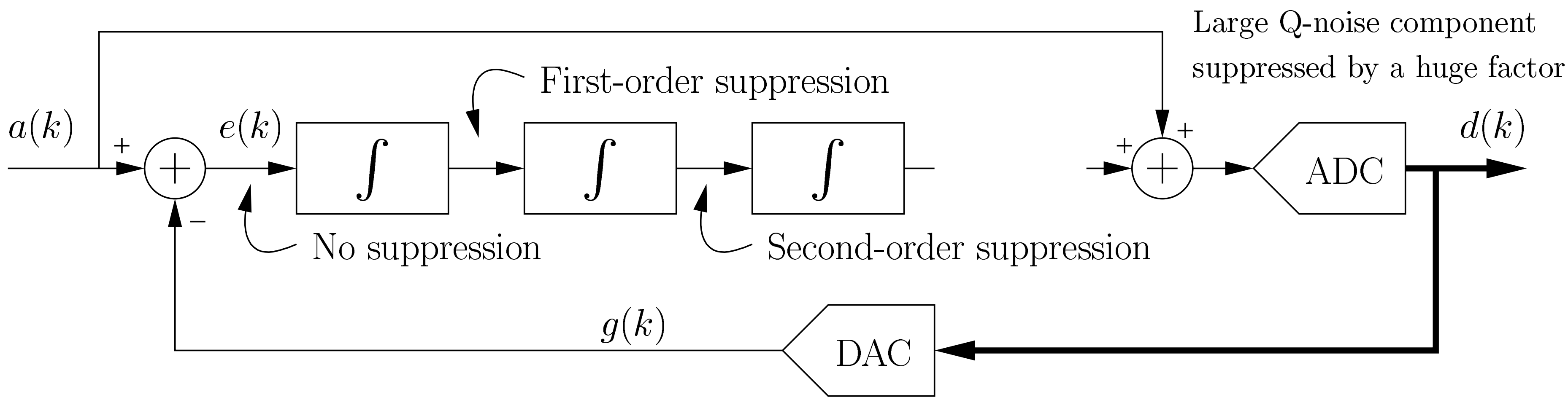
Quantization Noise (Quick Review)

Mismatch-Induced Noise

Noise Sources in a SC Delta-Sigma Modulator

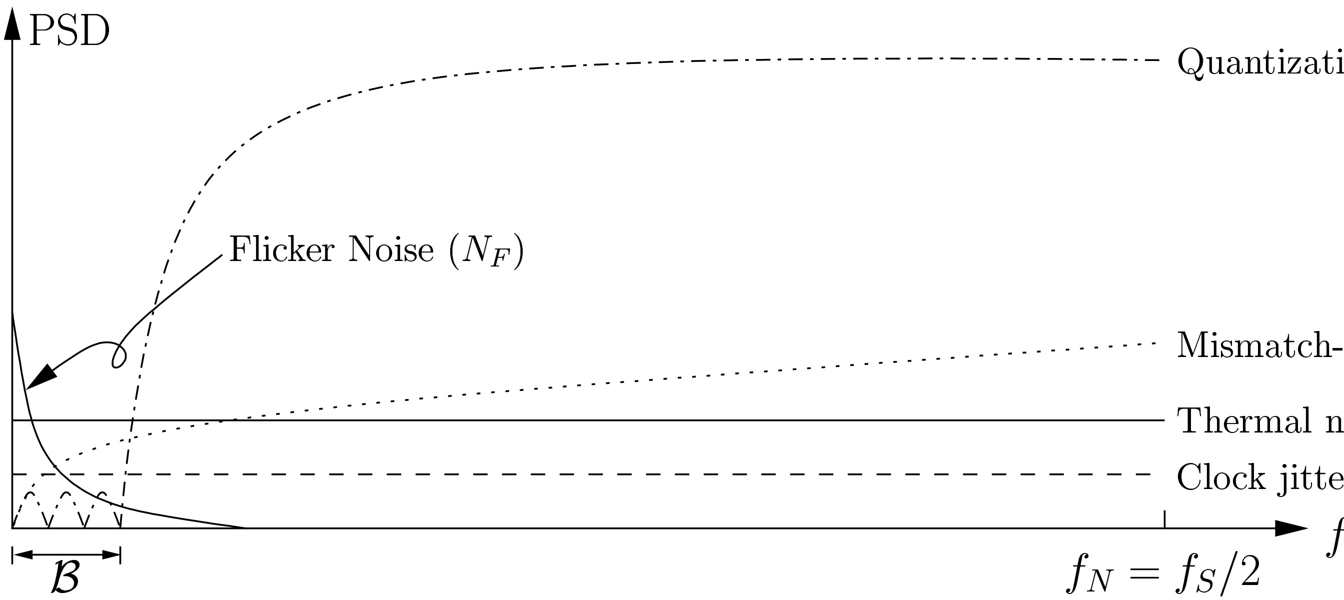


Nodes that are Sensitive to Imperfections



- ☞ To enable meaningful comparisons, all errors will be referred to the input
- ☞ The modulator's sensitivity to errors spans from "severe" to "negligible"
  - [!] Any errors, including noise, in $e(k)$ will adversely affect the performance
  - [!] Generating and subtracting $g(k)$ from $a(k)$ is a very critical process
  - ✔ Errors that occur in subsequent stages of the loop filter are of less concern, as they are suppressed by the gain from $e(k)$ to the respective node
  - ✔ The performance is virtually insensitive to errors that occur in the proposed feed-forward signal path (except when the OSR is extremely low)

Power Spectral Density of the Main Noise Sources

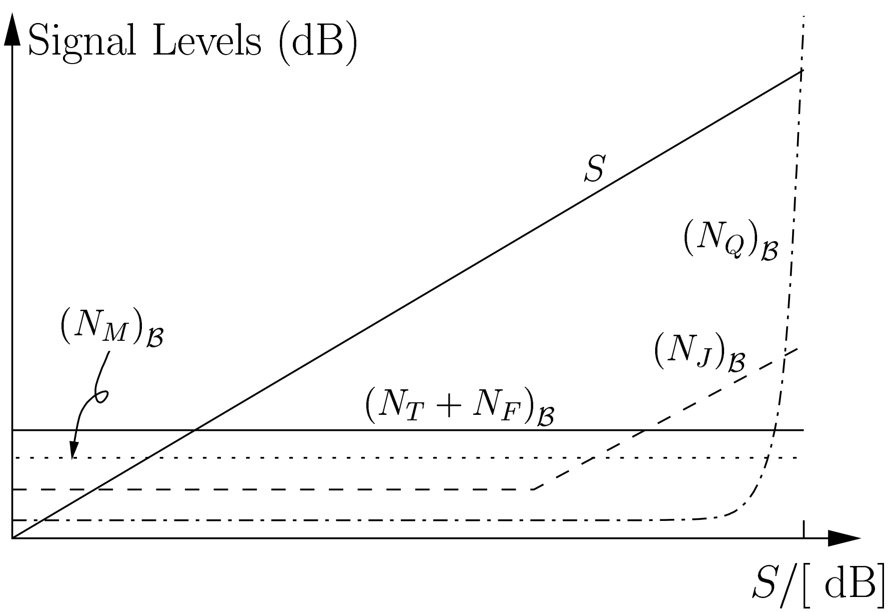


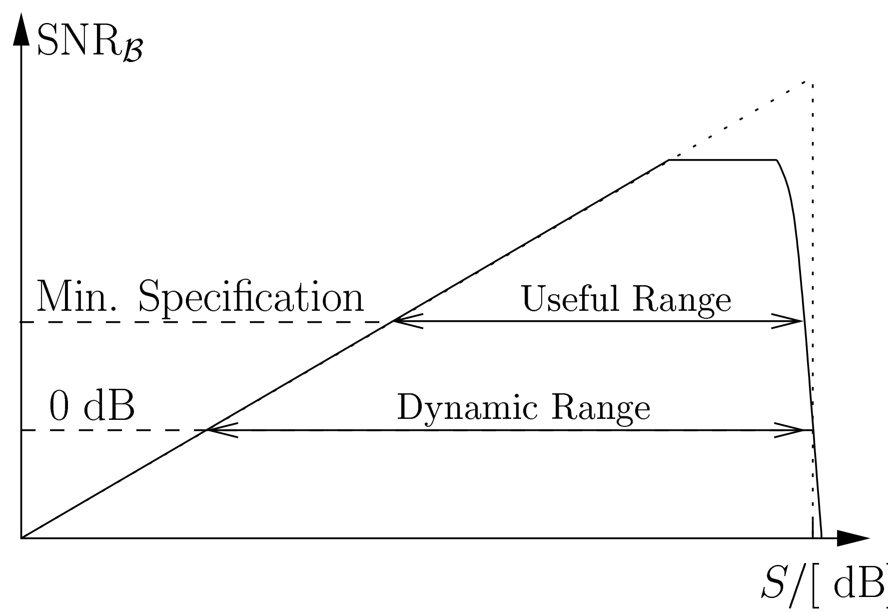
$$\left(\frac{S}{N}\right)_{\mathcal{B}} = \frac{S}{(N_Q)_{\mathcal{B}} + (N_T)_{\mathcal{B}} + (N_F)_{\mathcal{B}} + (N_J)_{\mathcal{B}} + (N_M)_{\mathcal{B}}}$$

☞ For SC implementations, $(N_T)_{\mathcal{B}}$ is inversely proportional to $\sqrt{\mathsf{OSR} \cdot C_{\mathsf{eff}}}$

- $\boxed{!}$ The power consumption is generally determined by $(N_T)_{\mathcal{B}}$
- $\boxed{!}$ Low power consumption: $(N_Q)_{\mathcal{B}} + (N_F)_{\mathcal{B}} + (N_J)_{\mathcal{B}} + (N_M)_{\mathcal{B}} < (N_T)_{\mathcal{B}}$
- $\boxed{!}$ When idle tones are expected, we want: $(N_Q)_{\mathcal{B}} + (N_M)_{\mathcal{B}} < (N_T)_{\mathcal{B}} - 20$ dB

Noise Components may Depend on the Input Signal





- ☞ N_T and N_F are generally (but not always) independent of the signal level S
  - ✘ Reducing N_T by 3 dB generally implies doubling the power consumption
  - ✔ N_F can often be reduced by using Chopper and/or CDS techniques
- $\boxed{!}$ N_Q is strongly signal-dependent for high signal levels S (stability issue)
- $\boxed{!}$ N_J depends on the derivative of the signal with respect to time
  - ✘ N_J is critical for modulators based on a continuous-time feedback signal

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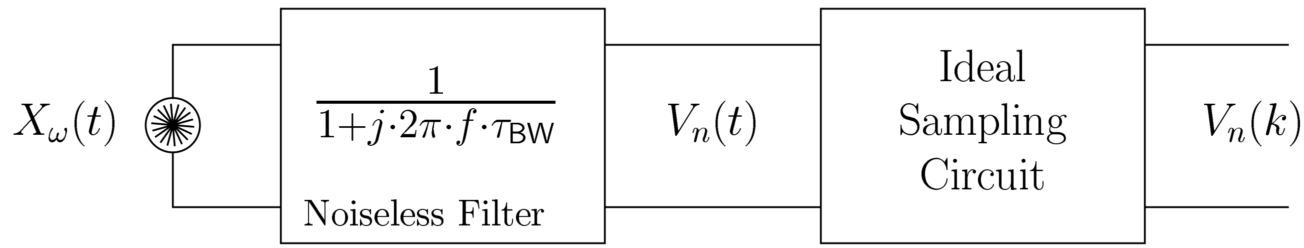
When Sampling a Single-Pole Noise Signal



- $X_\omega(t)$ is a theoretical white noise signal with infinite bandwidth, constant power spectral density PSD_{X_ω}, and hence has infinite power
- $V_n(t)$ is a filtered version of $X_\omega(t)$ using a single-pole low-pass filter with time constant τ_{BW} and 0dB gain in the pass band

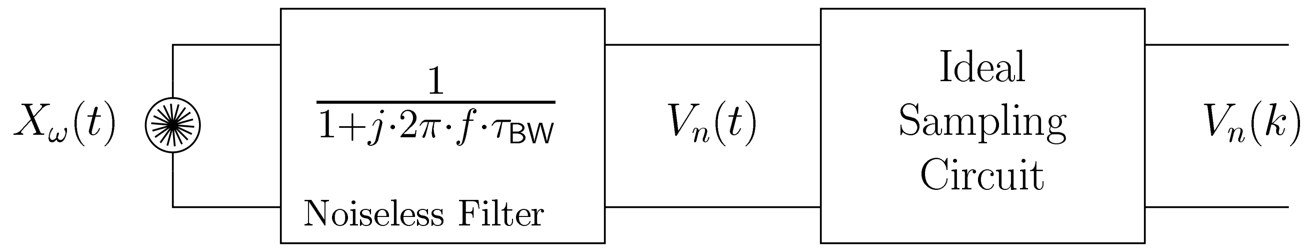
$$\mathsf{PSD}_{V_n(t)}(f) = \mathsf{PSD}_{X_\omega} \cdot |H(f)|^2 = \frac{\mathsf{PSD}_{X_\omega}}{1 + (2\pi f \tau_{BW})^2}$$

- The power of $V_n(t)$ is finite, which we can calculate as follows

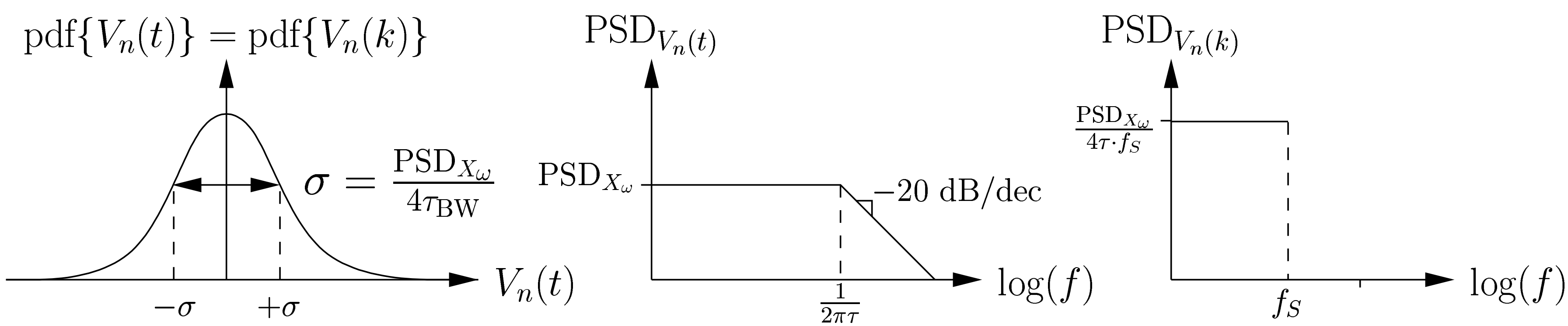
$$[V_n(t)]^2_{\mathsf{rms}} = \int_0^\infty \mathsf{PSD}_{V_n(t)}(f)df = \int_0^\infty \frac{\mathsf{PSD}_{X_\omega}}{1 + (2\pi f \tau_{BW})^2}df = \frac{\mathsf{PSD}_{X_\omega}}{4\tau_{BW}}$$

- This is a key result, which will be used repeatedly in this lecture

When Sampling a Single-Pole Noise Signal



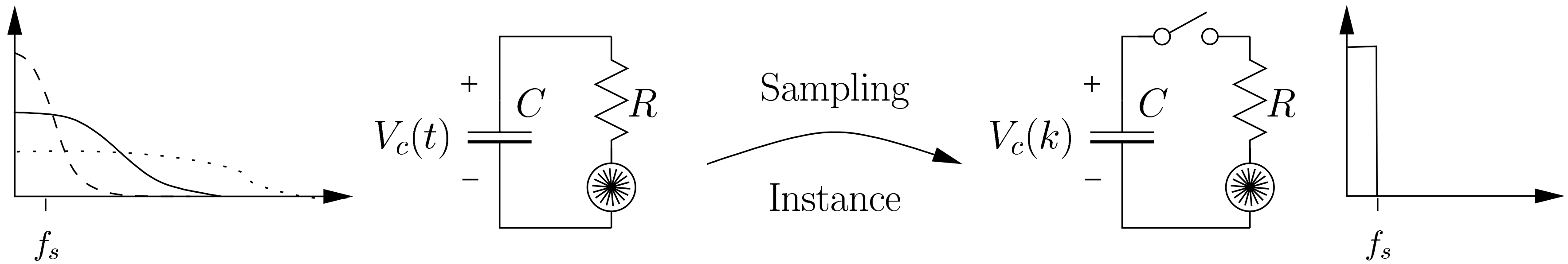
? Why is it that the pdf $V_n(k)$ is *exactly* the same as the pdf of $V_n(t)$?



! When the sampling period T_S is substantially greater (10x) than τ_{BW} there is virtually no correlation between one sample of $V_n(k)$ and the next, and *therefore* (in that case) $\mathrm{PSD}_{V_n(k)}(f)$ is essentially constant

$$\mathrm{PSD}_{V_n(k)} = \frac{[V_n(t)]^2_{\mathrm{rms}}}{f_S} = \frac{\mathrm{PSD}_{X_\omega}}{4\tau_{BW}\cdot f_S} \quad \text{and} \quad V_n(k) \in \mathcal{N}\left\{0, \frac{\mathrm{PSD}_{X_\omega}}{4\tau_{BW}}\right\}$$

Example Deriving the Famous "kT/C" Result



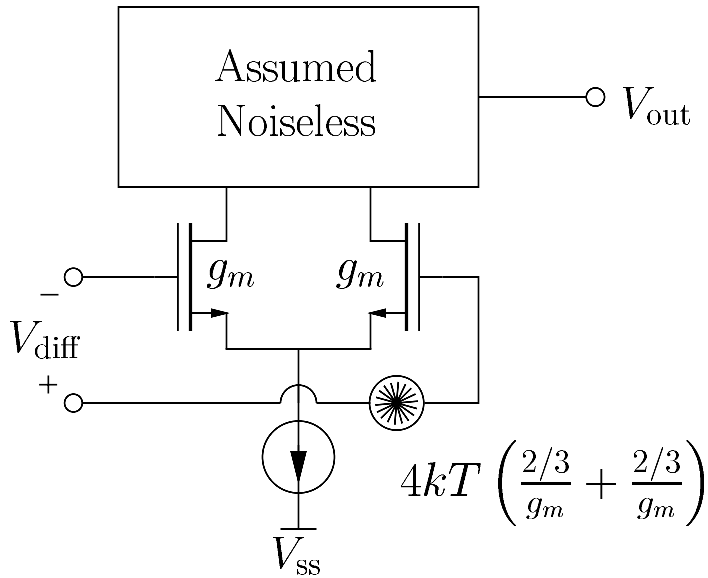
- The thermal noise component for the resistor is described by $\mathsf{PSD}_R = 4kTR$
- $V_c(t)$ is a first-order low-pass filtered version of the thermal noise
  - The filter's time constant is $\tau_{\mathsf{BW}} = R \cdot C$
  - The PSD of $V_c(t)$ at low frequencies is $4kTR$
- Utilizing the results we have derrived, we can now find very easily

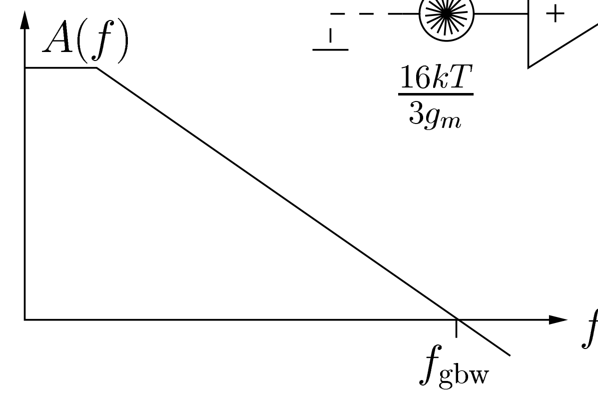
$$[V_c(t)]^2_{\mathsf{rms}} = \frac{\mathsf{PSD}_{V_c(t)}(f=0)}{4\tau_{\mathsf{BW}}} = \frac{4kTR}{4RC} = \frac{kT}{C}$$

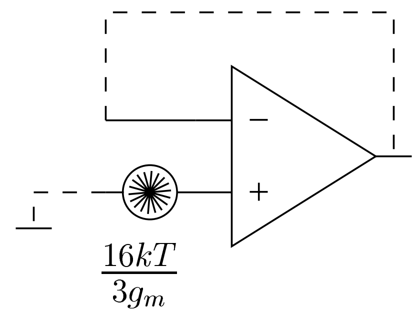
- Assuming $T_S \geq 10 \cdot RC$, we know that $V_c(k)$ and $V_c(k+1)$ are uncorrelated, and hence

$$[V_c(k)]^2_{\mathsf{rms}} = [V_c(t)]^2_{\mathsf{rms}} = \frac{kT}{C} \quad \text{and} \quad \mathsf{PSD}_{V_c(k)} = \frac{kT}{Cf_S}$$

Thermal Noise in Operational Amplifiers

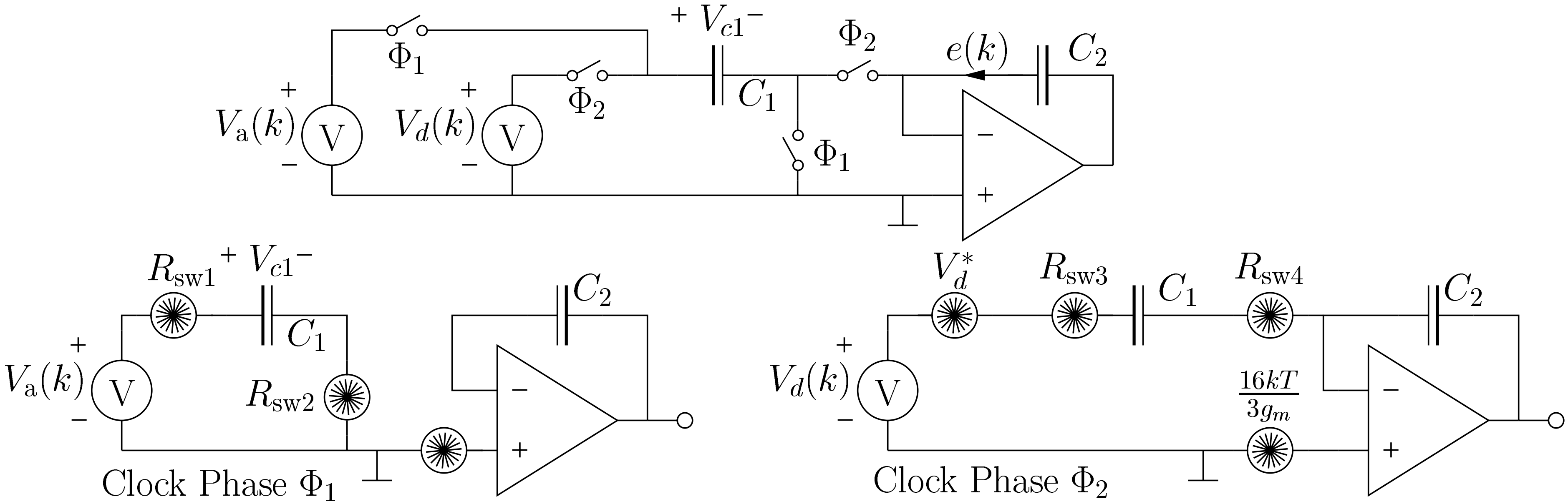






- ☞ All transistors contribute to the input-referred thermal noise
  - ! When designed for low-noise, the diff-pair transistors should dominate
  - ! In that case, the input-referred noise's PSD will be approximately $\frac{16kT}{3g_m}$
  - ✘ Low noise generally implies high power consumption (because $g_m \propto I_d$)
- ☞ You can use SPICE to determine the input-referred noise level of your opamp in a continuous-time configuration, e.g., a unity-gain configuration
  - ! The objective is to determine the noise when used in a SC DSM application

Thermal Noise in the Input Stage of a SC DSM



☞ The calculations are derived most effectively by first focusing on $e(k)$

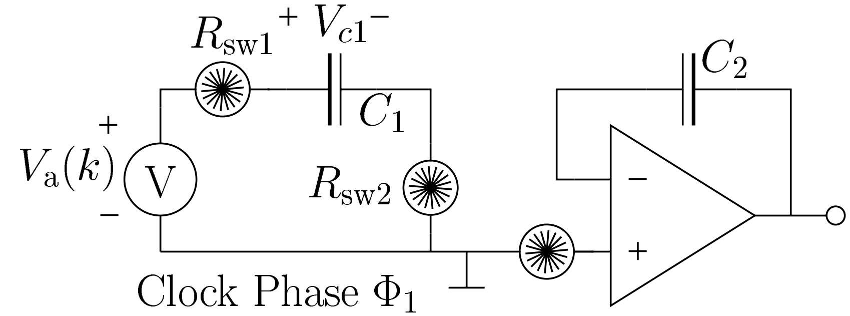
- $e(k)$ is the charge pulse signal being integrated $V_{\text{out}}(k) = \frac{1}{C_2} \cdot \sum_{i=0}^{k} e(i)$

☞ The desired/signal component in $e(k)$ is $e_s(k) = C_1 \cdot [V_a(k) - V_d(k)]$

☞ Once we have calculated the thermal noise component $e^*(k)$ in $e(k)$, we may refer it back to the input signal as follows

$$\text{SNR} = \frac{[V_a(k)]_{\text{rms}}}{e^*(k)/C_1}$$

Thermal Noise Analysis – Clock Phase Φ_1



- ☞ Nominally, the voltage signal $V_a(k)$ is stored on the capacitor C_1
- ☞ Thermal noise due to resistance in the switches will unavoidably cause stochastic variations in $V_{c1}(k) - V_{\mathsf{a}}(k)$
- ☞ Deterministic effects, such as non-stochastic charge injection, should be counted as offset contributions, and not as noise contributions
- ☞ Noise stored as voltage/charge on capacitor C_1 will cause a charge transfer $e(k)$ in the same manner as charge transfer caused by the input signal $V_a(k)$

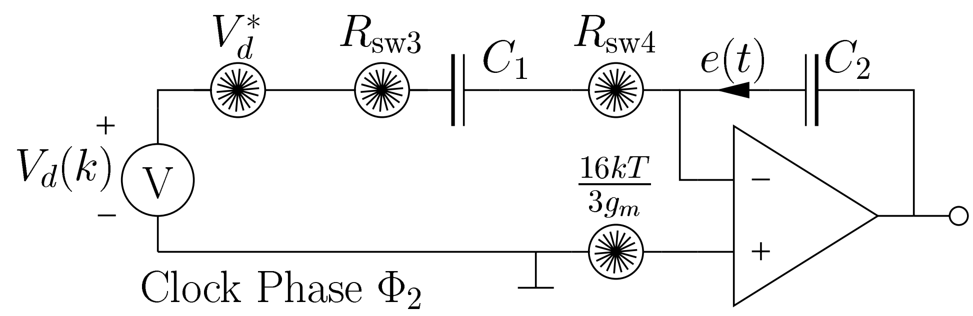
$$\left[e^*_{\mathsf{sw1,sw2}}\right]^2_{\mathsf{rms}} = \frac{4kTR \cdot C_1^2}{4\tau_{\mathsf{BW}}} = \frac{4kTRC_1^2}{4RC_1} = kTC_1, \quad \text{where} \quad R = R_{\mathsf{sw1}} + R_{\mathsf{sw2}}$$

$\boxed{!}$ Alternatively, we may express the result in the voltage domain

$$[V_{n1}(k)]^2_{\mathsf{rms}} = [V_{c1}(t) - V_{\mathsf{a}}(k)]^2_{\mathsf{rms}} = \frac{\mathsf{PSD}(0)}{4\tau_{\mathsf{BW}}} = \frac{4kT(R_{\mathsf{sw1}} + R_{\mathsf{sw2}})}{4C_1(R_{\mathsf{sw1}} + R_{\mathsf{sw2}})} = \frac{kT}{C_1}$$

Thermal Noise Analysis – Clock Phase Φ_2

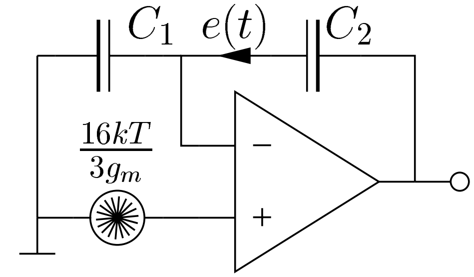
- There is a lot going on in phase Φ_2, so we will cover it piecemeal
- It is necessary to first consider the continuous-time dynamics of $e(t)$



- The time constant τ_{BW} by which the system settles is determined by the bandwidth of the opamp and the feeback factor β
  - ! There is not a fundamental relationship between τ_{BW} and the noises' PSD
  - ! Do not blindly assume that all noise contributions are the form kT/C
- τ_{BW} can be determined quite easily using SPICE (plot the current $\frac{d}{dt}(e(t))$)
- For any design, however, you have an apriori knowledge of the value of τ_{BW}
  - ! The system must settle to N bits of precision within 1 of q clock phases

$$\frac{1}{\tau_{BW}} \geq N \cdot \ln(2) \cdot q \cdot f_S \quad \text{(add some margin for slewing etc.)}$$

Thermal Noise Analysis – Opamp



- Use continuous-time simulations to find/estimate the parameters $\tau_{\text{BW}} \simeq \frac{1}{30 f_S}$ and $\text{PSD}_{\text{AMP}} \simeq \frac{16kT}{3g_m}$
- Two-stage opamps, e.g., do not have a fundamental relationship between g_m and τ_{BW} (optimize)
- Based on the (very reasonable) assumption that you have designed the system to have a first-order settling behavior (characterized by τ_{BW}) we find that

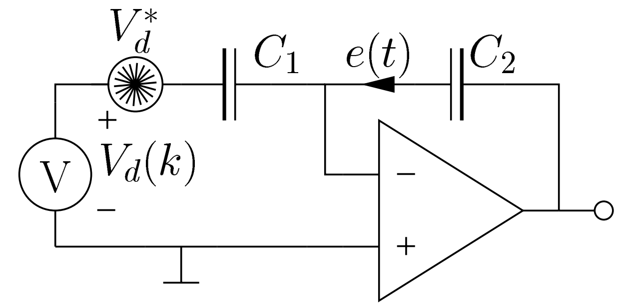
  $\boxed{!}$ $e(t)$ comprises a stochastic component which effectively is a first-order low-pass filtered white noise signal having a total power of

$$[e^*_{\text{AMP}}(t)]^2_{\text{rms}} = \frac{\text{PSD}_{e,\text{AMP}}}{4\tau_{\text{BW}}} = \frac{C_1^2 \cdot \text{PSD}_{\text{AMP}}}{4\tau_{\text{BW}}} \simeq \frac{C_1^2 \cdot 40kT f_S}{g_m}$$

- Given that the system settles fully $\tau_{\text{BW}} \simeq \frac{1}{30 f_S}$ we deduce that there is virtually no correlation between one sample of $e^*(t)$ and the next, and hence we conclude that $e^*_{\text{AMP}}(k)$ is a white noise signal $e^*_{\text{AMP}}(k) \in \mathcal{N}\left\{0, \frac{C_1^2 \cdot \text{PSD}_{\text{AMP}}}{4\tau_{\text{BW}}}\right\}$

$\boxed{!}$ Do not use a opamp that is faster than necessary $\rightarrow$ significant noise penalty

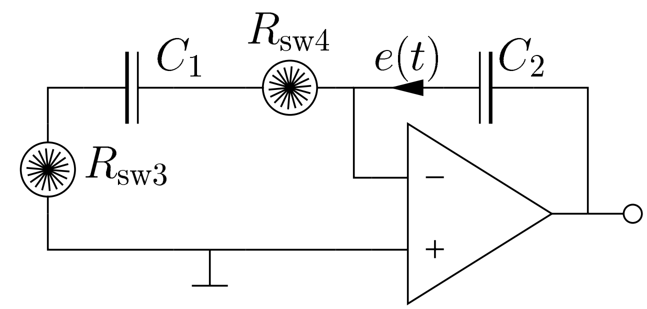
Thermal Noise Analysis – Voltage Reference



- A similar method can be used to estimate the thermal noise contribution from the reference voltage buffer (used to implement the DAC)
- The referenece voltage buffer can be designed in several different ways, and the noise characteristics may be very different
  - ! A fast voltage reference buffer facilitates full integration, but care must be taken to assure proper "single-pole" settling $[e^*(k)]^2_{\text{rms}} = \frac{C_1^2 \cdot \text{PSD}_{\text{REF}}}{4\tau_{\text{BW}}}$
  - ! Some designs use a slow reference-voltage amplifier driving a large external capacitor (then the bandwidth of $e^*(t)$ is not determined by opamp)
- If the dynamics of the noise component induced in $e(t)$ by the reference voltage buffer do not meet the assumptions for the previously derrived result:
  - ! use SPICE to estimate the PSD of the induced noise signal $e^*(t)$

$$[e^*(k)_{\mathcal{B}}]^2_{\text{rms}} = \int_{f_{\mathcal{A}}} \text{PSD}_{e^*(t)} df$$ where $f_{\mathcal{A}}$ are the "aliasing" frequencies

Thermal Noise Analysis – Switches 3 and 4



☞ This situation is potentially very deceiving

☞ The induced noise's PSD at low frequencies is $\text{PSD}_{e^*(t)} = C_1^2 \cdot 4kT(R_{\text{sw3}} + R_{\text{sw4}})$

☞ The bandwidth can be estimated in the manner described earlier: $\tau_{\text{BW}} \simeq \frac{T_S}{30}$

☞ We may thus (correctly) estimate that $[e(t)]^2_{\text{rms}} = \frac{\text{PSD}_{e(t)}}{4\tau_{\text{BW}}} \simeq kTC_1 \cdot \frac{30C_1R}{T_S}$

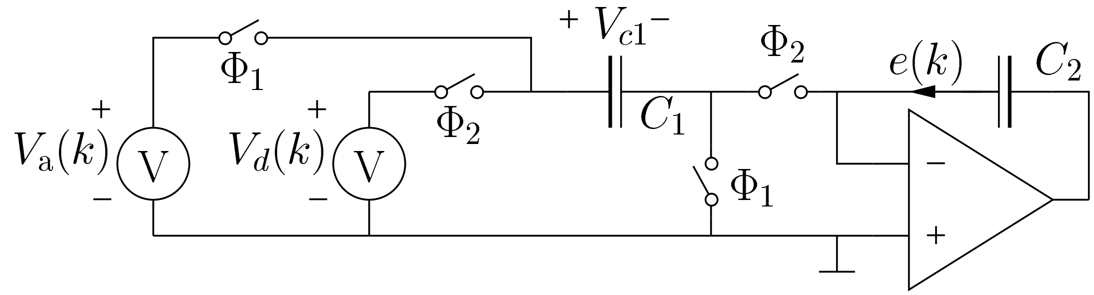
- ✔ By choosing $R_{\text{sw3}}+R_{\text{sw4}}$ sufficiently small, we can achieve $[e(t)]^2_{\text{rms}} \leq kTC_1$
- ✘ The result is valid only in steady state when the switches are closed

! During the on-to-off transition, the carriers are "slowly" (on a fS time scale) diffusing away from the inverted MOSFET channel

- ! The switches' impedance and PSD is thus increased gradually, and the system's bandwidth will eventually be limited by the switches' impedance

$$[e(k)]^2_{\text{rms}} = \lim_{t \to kT_s} \left[\frac{\text{PSD}_{e(t)}}{4\tau_{\text{BW}}} \right] = \frac{4kTC_1^2(R_{\text{sw3}} + R_{\text{sw4}})}{4C_1(R_{\text{sw3}} + R_{\text{sw4}})} = kTC_1$$

Thermal Noise Analysis – Summary



☞ The signal component comprised in $e(k)$ is $e_s(k) = C_1 \cdot (V_a(k) - V_d(k))$

☞ The cummulative white noise component comprised in $e(k)$ is

$$[e^*(k)]^2_{\mathsf{rms}} = kTC_1 + \frac{C_1^2 \cdot \mathsf{PSD}_{\mathsf{AMP}}}{4\tau_{\mathsf{BW}}} + \frac{C_1^2 \cdot \mathsf{PSD}_{\mathsf{REF}}}{4\tau_{\mathsf{BW}}} + kTC_1$$

✔ Only a fraction $\frac{1}{\mathsf{OSR}}$ of the power in $[e^*(k)]^2_{\mathsf{rms}}$ is located in the signalband

☞ The signal-band SNR can thus be calculated as

$$\mathsf{SNR}_{\mathcal{B}} = \frac{[V_a(k)]_{\mathsf{rms}}}{\frac{[e^*(k)]_{\mathsf{rms}}}{C_1\sqrt{\mathsf{OSR}}}} = \frac{[V_a(k)]_{\mathsf{rms}}}{\sqrt{\frac{2kT}{C_1\mathsf{OSR}} + \frac{\mathsf{PSD}_{\mathsf{AMP}}+\mathsf{PSD}_{\mathsf{REF}}}{4\tau_{\mathsf{BW}}\mathsf{OSR}}}} \simeq \frac{[V_a(k)]_{\mathsf{rms}}}{\sqrt{\frac{kT}{\mathsf{OSR}} \cdot \left(\frac{2}{C_1} + \frac{8}{3 \cdot g_m \tau_{\mathsf{BW}}}\right)}}$$

☞ Note that $g_m \cdot \tau_{\mathsf{BW}}$ is a capacitance. Typically $\sqrt{\frac{3kT}{\mathsf{OSR} \cdot C_1}} < (N_T)_{\mathcal{B}} < \sqrt{\frac{5kT}{\mathsf{OSR} \cdot C_1}}$

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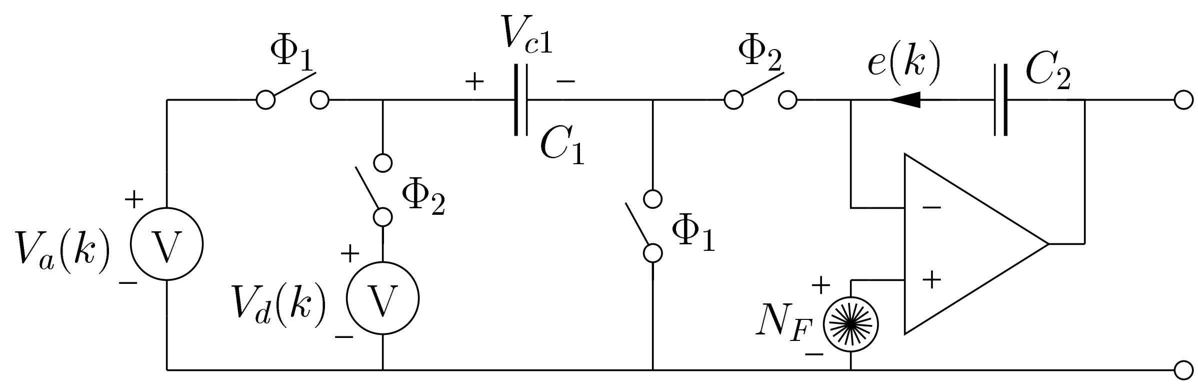
Flicker Noise - A Problem in CMOS



☞ We may calculate the charge being integrated as

$$\begin{aligned} e(k) &= -C_1 \cdot \Delta V_{c1}(k) = C_1 \cdot ([V_\mathsf{a}(k) - 0] - [V_d(k) - N_F(k)]) \\ &= C_1 \cdot ([V_\mathsf{a}(k) - V_d(k)] + [N_F(k) - 0]) \end{aligned}$$

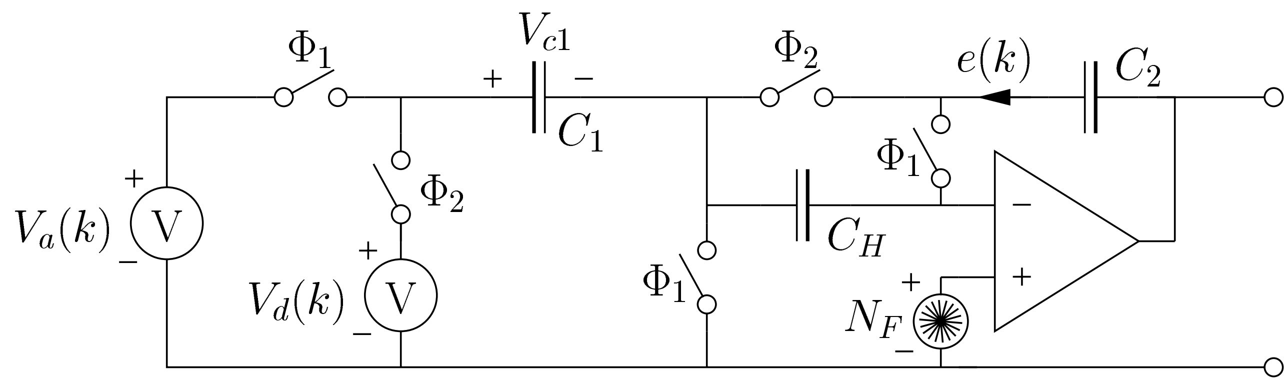
- ✘ Flicker noise enters the system in the same way as $V_\mathsf{a}(k)$
- ✘ Reducing N_F may be expensive in terms of power and/or chip area

☞ Ideally, the voltage variation on the capacitor's right-hand side would be zero

- $\boxed{!}$ We can obtain this behavior by replacing 0 by $N_F(k)$, or vice versa

☞ N_F is low-frequency noise: $N_F(k) \simeq N_F(k+1)$

Correlated Double Sampling (CDS) Techniques



☞ This basic CDS scheme was originally proposed by K. Nagaraj
"SC Circuits with reduced sensitivity to finite amplifier gain," Proc. for IEEE Int. Symp. for Circuits and Systems, pp. 618–621, 1986

☞ Essentially, C_H stores the offset and flicker noise component

$$e(k) \; = \; C_1 \cdot \left([V_{\mathsf{a}}(k) - V_d(k)] + (N_F(k) - N_F(k - \tfrac{1}{2})) \right)$$

✔ Because N_F is low-frequency noise, we have $(N_F(k) - N_F(k - \frac{1}{2})) \simeq 0$

☞ The power consumption is increased

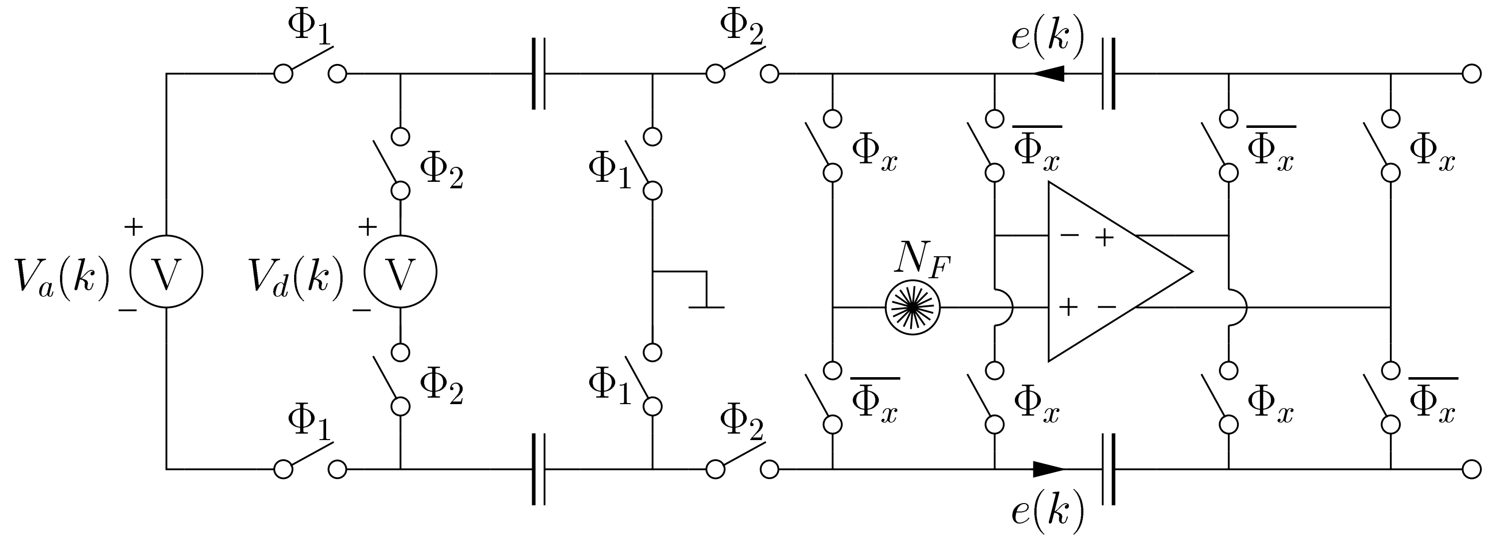
✘ The opamp's thermal noise is sampled twice (same for all CDS schemes)

✘ C_H should be significantly larger than C_1 to minimize the noise penalty

✘ CDS topologies do not support double-sampling operation

✔ Certain CDS schemes have substantial advantages for highly nonlinear opamps
"Jesper Steensgaard, "Nonlinearities in SC Delta-Sigma A/D Converters," IEEE Int. Conf. on Elec. Circuits Syst. pp. 355, Sept. 1998.

Chopper Suppression of Flicker Noise



☞ Chopping techniques are best known for their use in continuous-time circuits

- ! This is surprising because such techniques are *ideal* for SC circuits
- ✔ Simply "rotate" the diff. opamp in every clock period: $\Phi_x = 1$ for k even
- ✔ There is no thermal noise penalty
- ✔ A high sampling frequency can be achieved (double sampling is also feasible)
- ✔ N_F is modulated to $f_S/2$; it is filtered out in the decimation process

☞ Although first published in 1981, it has not been used "widely" until recently

K. Hsieh, P. Gray, D. Senderowich, and D. Messerschmitt, IEEE Journal of Solid-State Circuits, vol. SC-16, pp. 708–715, Dec. 1981
C. Wang, R. Castello, and P. Gray, IEEE Journal of Solid-State Circuits, vol. SC-21, pp. 57–64, Feb. 1986
T. Burger and Qiuting Huang., IEEE Solid-State Circuit Conference, Digest of Tech. Papers vol. 44, pp. 44-45, Feb. 2001

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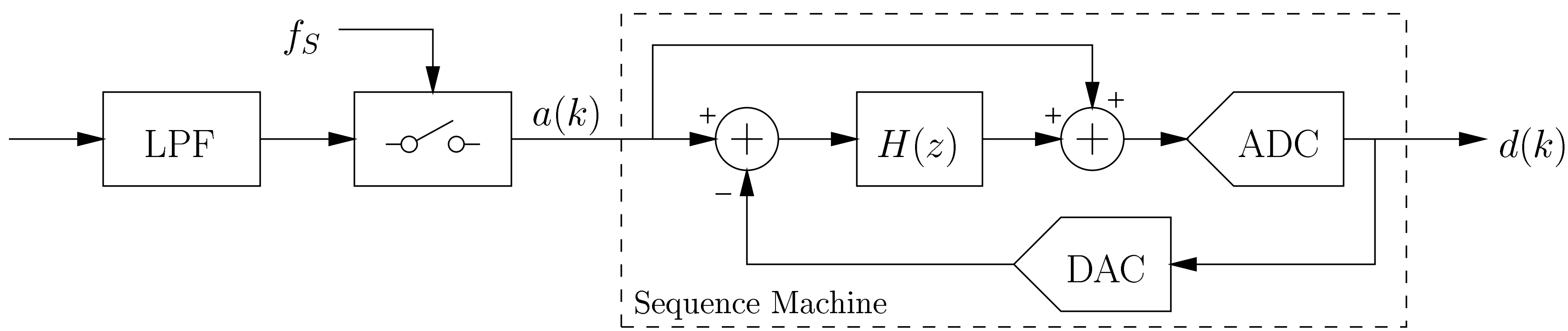
Clock Jitter Induced Noise in DT Modulators



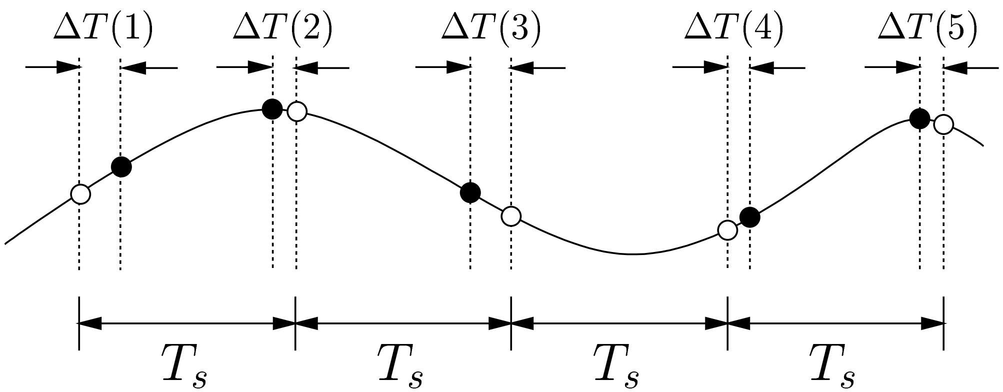
☞ Discrete-time (DT) signal processing is implemented by sequence machines

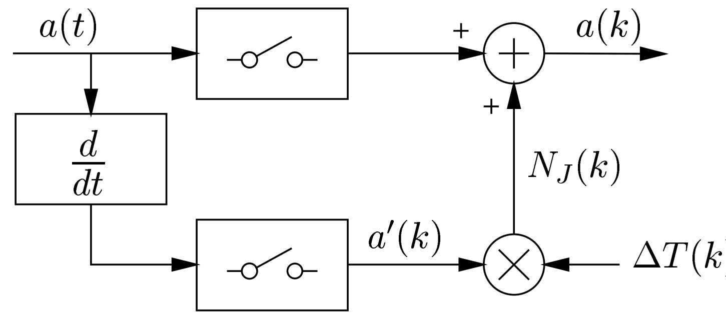
- ! Sequence machines can be either analog, digital, or both
- ! The signal is a *sequence* of values with no inherent correlation with time
- ✔ Hence, only the sampling process is sensitive to clock jitter

☞ To avoid *aliasing errors*, we need to filter a CT signal prior to sampling it

- ! The anti-aliasing filter's complexity is inversely related to the OSR
- ✘ The anti-aliasing filter must as linear and low-noise as the modulator
- ! OSRs of less than 10 are generally not very practical (any SC/SI circuit)

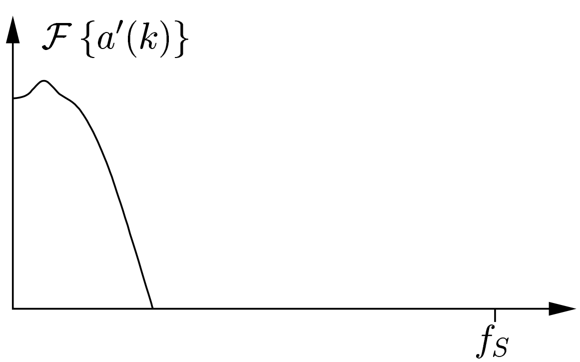
When Sampling a Signal – Broadband Jitter

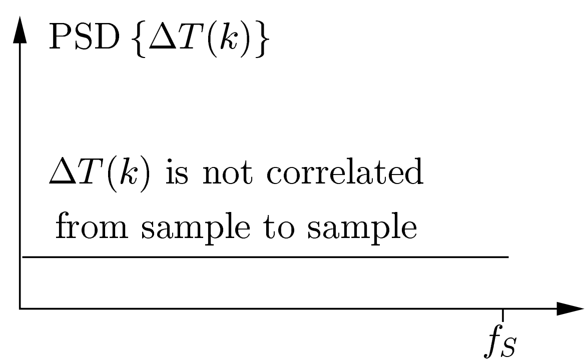


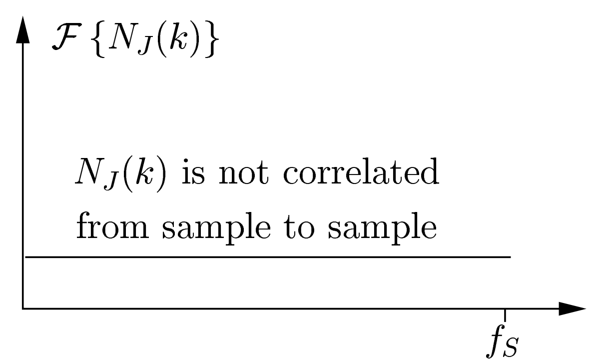


- The processing of $a(k)$ assumes that $a(t)$ is sampled uniformly (circles)
- A small uncertainty (jitter) in when each sample is taken may be modeled as an additive error (tangent approximation is not valid for large $\Delta T(k)$)

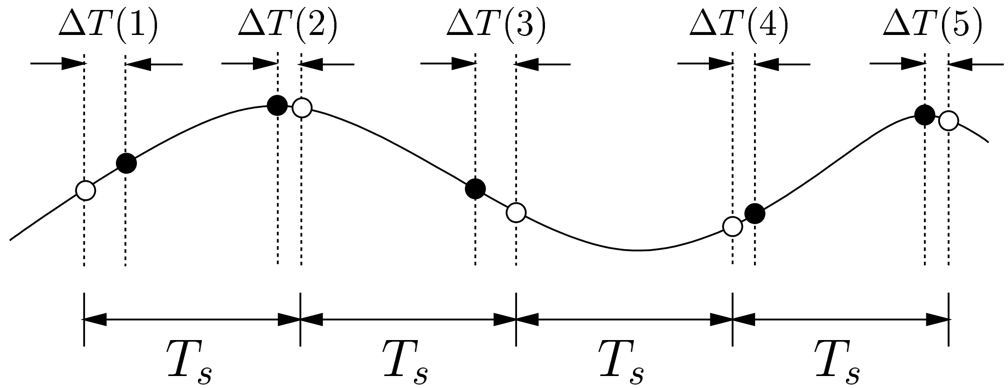
$$N_J(k) = \frac{d}{dt}\left[a(k \cdot T_s)\right] \cdot \Delta T(k)$$

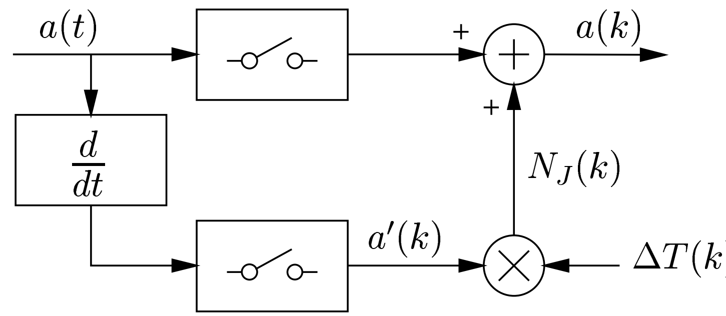






Estimating the Power of $N_J(k)$





☞ The system is most sensitive to clock jitter when $|\frac{d}{dt}a(t)|$ is large

☞ We will thus consider a tone at the edge of the base band:

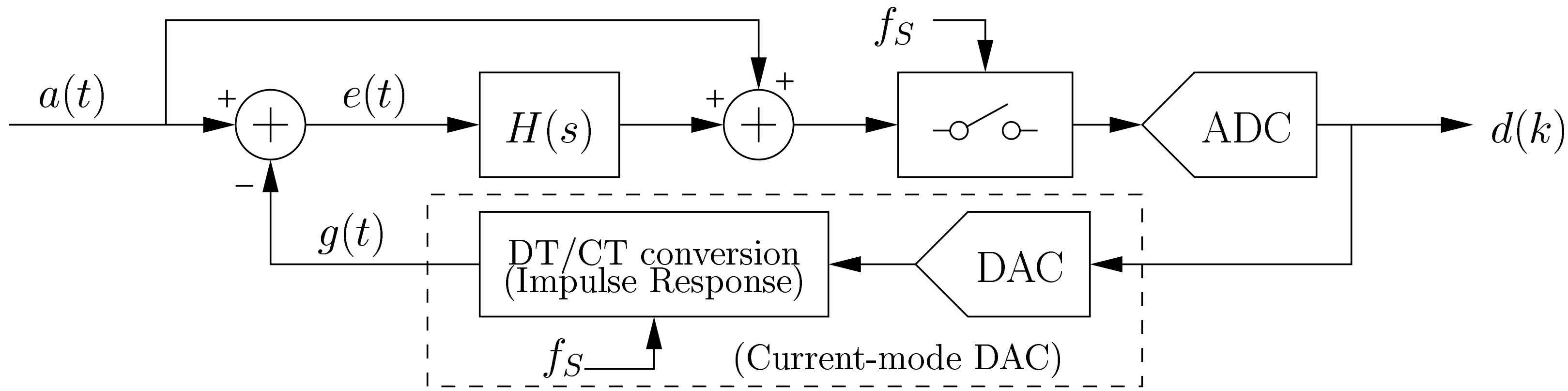
$$\begin{aligned}[N_J(k)]_{\mathsf{rms}} &= \left[A_0 \cdot 2\pi \frac{f_S}{2\mathsf{OSR}} \cdot \sin\left(2\pi \cdot \frac{f_S}{2\mathsf{OSR}} \cdot t\right)\right]_{\mathsf{rms}} \cdot [\Delta T(k)]_{\mathsf{rms}} \\ &= \frac{A_0}{\sqrt{2}} \cdot \frac{\pi}{\mathsf{OSR}} \cdot \frac{[\Delta T(k)]_{\mathsf{rms}}}{T_s} \quad \text{where typ.} \quad 10^{-5} \underset{\mathsf{xtal}}{<} \frac{[\Delta T(k)]_{\mathsf{rms}}}{T_s} \underset{\mathsf{relax}}{<} 10^{-2}\end{aligned}$$

✔ Calculating the in-band signal-to-noise ratio, we find (independent of A_0)

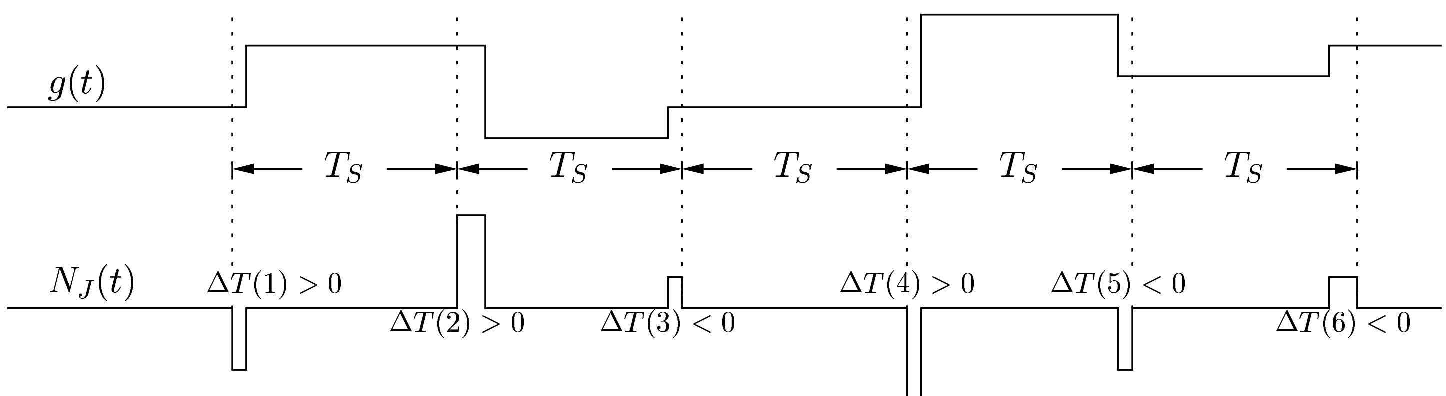
$$(\mathsf{SNR})_{\mathcal{B}} = \frac{A_0/\sqrt{2}}{[N_J(k)]_{\mathsf{rms}}/\sqrt{\mathsf{OSR}}} = \frac{\sqrt{\mathsf{OSR}^3}}{\pi} \cdot \frac{T_s}{[\Delta T(k)]_{\mathsf{rms}}} \underset{\mathsf{typ.}}{>} 100\ \mathsf{dB}$$

✘ It is quite a different story for band-pass modulators

Clock Jitter Induced Noise in CT Modulators

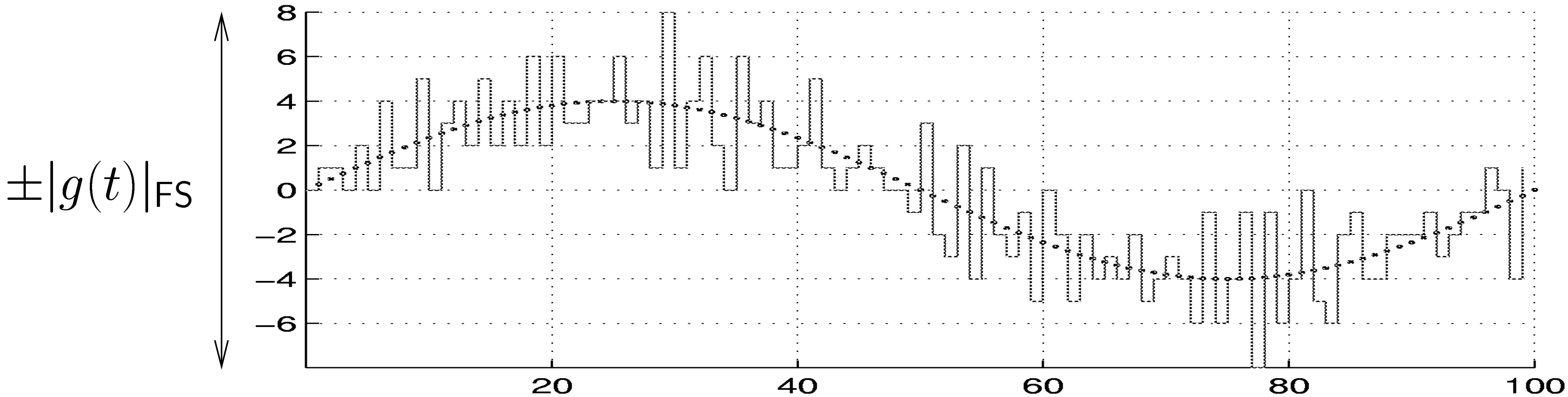


- ☞ Errors induced by clock jitter will occur only in the DT/CT/DT interfaces
  - ✔ Errors induced in the S/H process will be suppressed by NTF(z)
  - ✘ Errors caused by the feedback DAC will not be suppressed



$$[N_J(t)]^2_{\mathsf{rms}} = \lim_{T\to\infty} \frac{1}{2T} \int_{-T}^{T} N_J^2(t)dt = [K_{\mathsf{dac}} \cdot \Delta d(k)]^2_{\mathsf{rms}} \cdot \left[\frac{\Delta T(k)}{T_S}\right]^2_{\mathsf{rms}}$$

Clock Jitter Induced Noise in CT Modulators



- $K_{\mathsf{dac}} \cdot \Delta d(k)$ will be an integer number of g_{LSB} where for an N-level quantizer

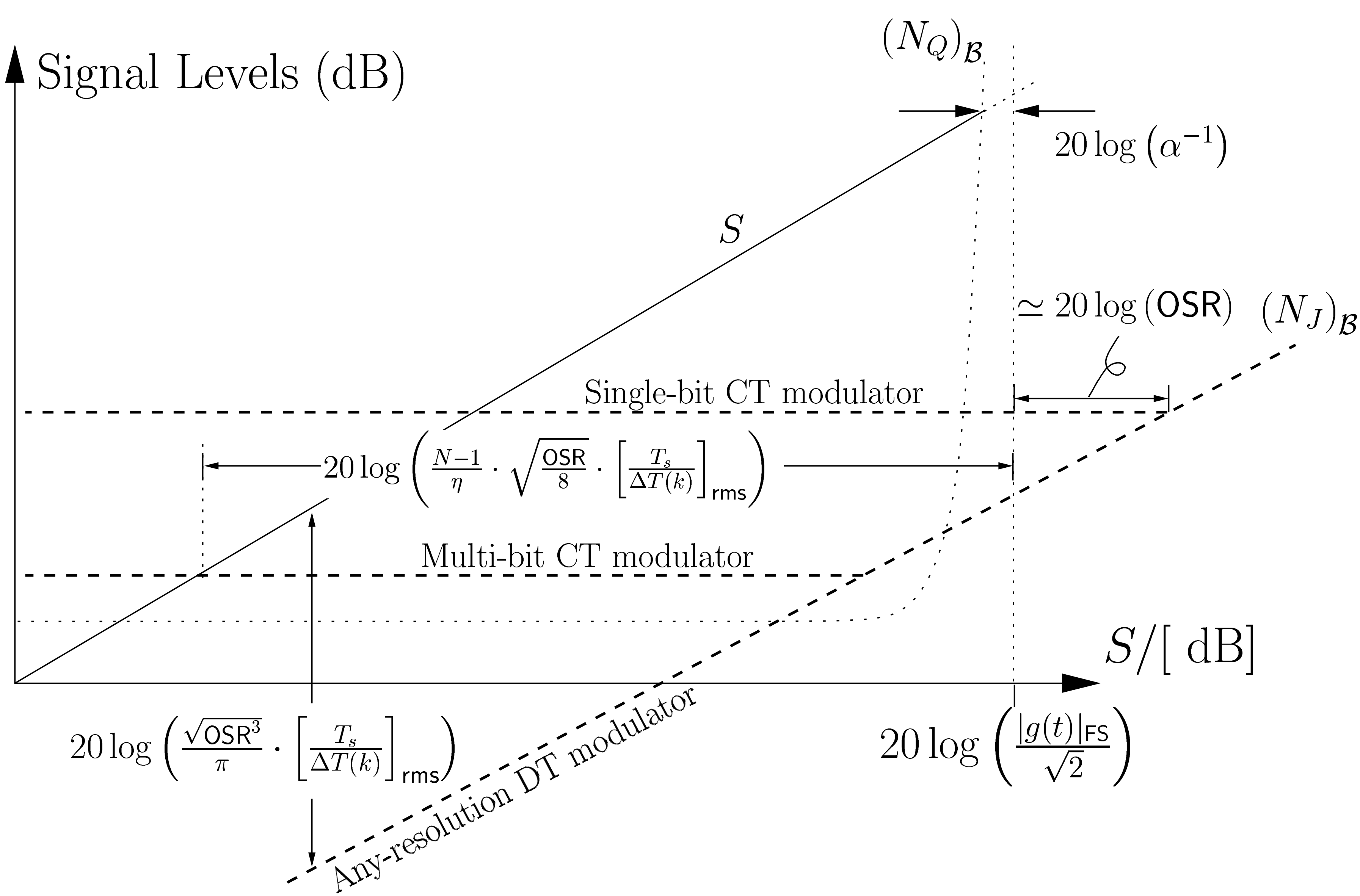
$$(N-1) \cdot g_{\mathsf{LSB}} = 2 \cdot |g(t)|_{\mathsf{FS}}$$

- Let $\alpha = \frac{|a(t)|_{\mathsf{FS}}}{|g(t)|_{\mathsf{FS}}}$ and $\eta \cdot g_{\mathsf{LSB}} = [K_{\mathsf{dac}} \cdot \Delta d(k)]_{\mathsf{rms}}$ for $a(t) = 0$; and we find

$$(\mathsf{DR})_{\mathcal{B}} = \frac{\frac{|a(t)|_{\mathsf{FS}}}{\sqrt{2}}}{\frac{[N_J(t)]_{\mathsf{rms}}}{\sqrt{\mathsf{OSR}}}} = \frac{\alpha \cdot \frac{N-1}{2} \cdot \frac{g_{\mathsf{LSB}}}{\sqrt{2}}}{\frac{\eta \cdot g_{\mathsf{LSB}}}{\sqrt{\mathsf{OSR}}} \cdot \left[\frac{\Delta T(k)}{T_S}\right]_{\mathsf{rms}}} = \frac{\alpha}{\eta} \cdot (N-1) \cdot \sqrt{\frac{\mathsf{OSR}}{8}} \cdot \left[\frac{T_S}{\Delta T(k)}\right]_{\mathsf{rms}}$$

- For a conservatively designed modulator $H_\infty = 1.5$ we have $\alpha \simeq \eta \simeq 1$
- For an aggressively designed modulator $\eta \gg 1$ and $\alpha < 1$, you will need either a very good crystal clock and/or a high-resolution signal representation N

Clock Jitter Induced Noise – Summary

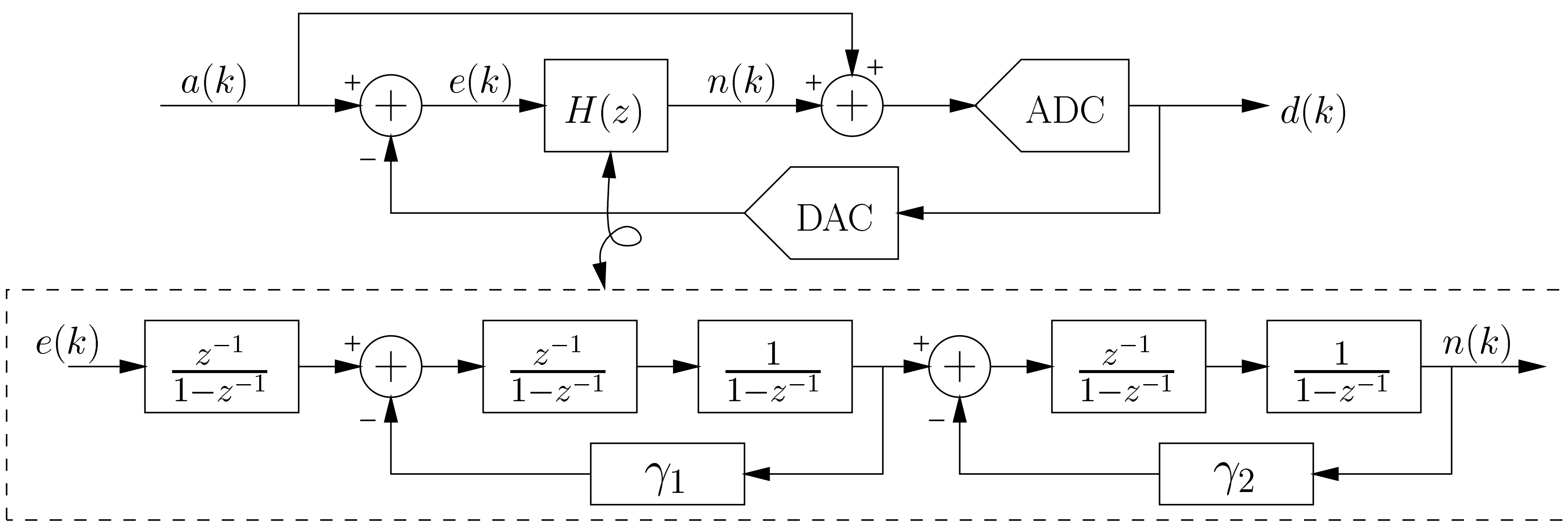


Outline – Progress

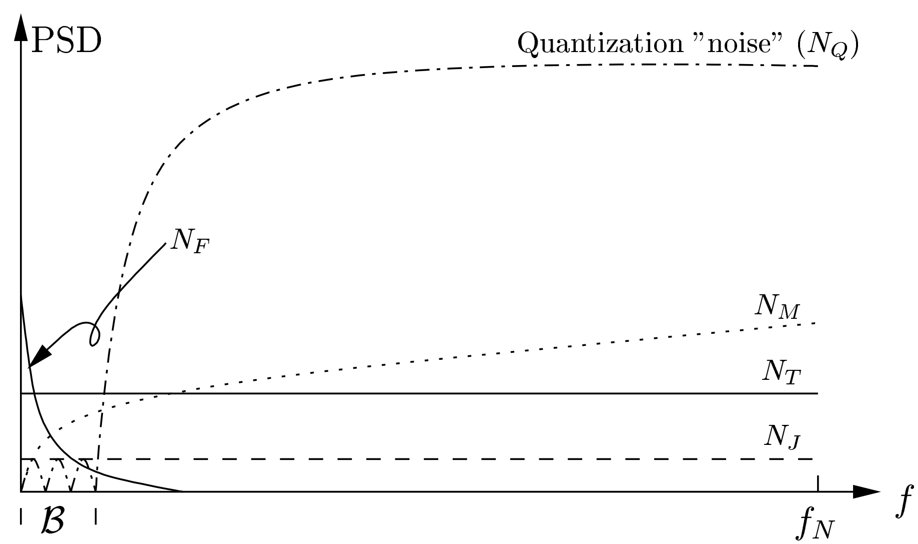
Noise Source in SC Delta-Sigma Modulators

- ✔ General Overview of Noise Sources in Delta-Sigma Modulators
- ✔ Thermal Noise
- ✔ Flicker Noise (CDS, Chopper Techniques)
- ✔ Clock Jitter Induced Noise (DT and CT Systems)
- ☞ Quantization Noise (Quick Review)
- Mismatch-Induced Noise

How to Suppress N_Q in the Signal Band



- Assuming $\text{PSD}_{n(k)}$ is bounded (system must be made stable), all we need is a loop filter with very high gain in the signal band
- Tradeoff between suppression of $(N_Q)_{\mathcal{B}}$ and the maximum input amplitude – affects dynamic range



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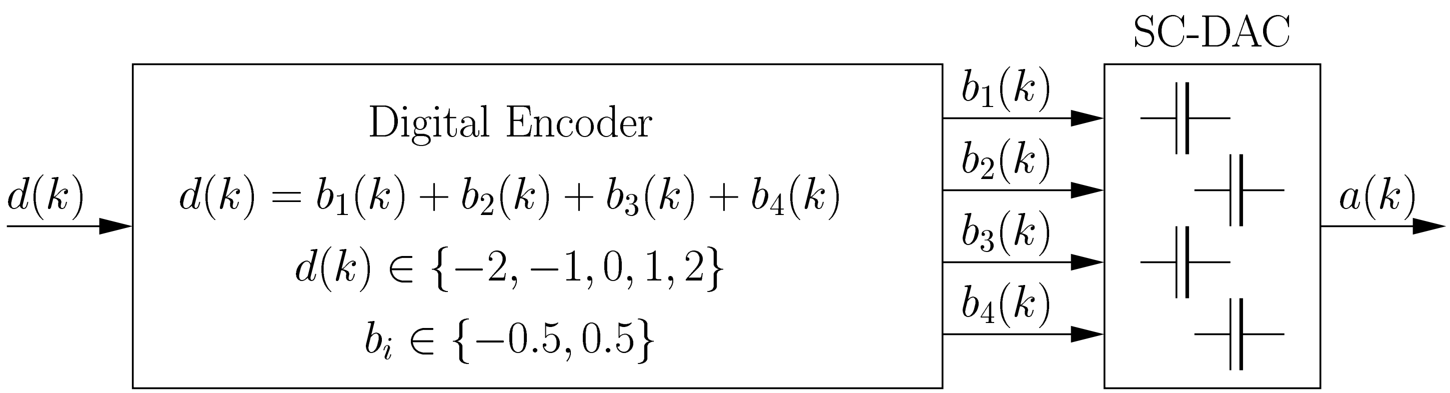
Randomizing Mismatch Errors

☞ Suppose we, for each new value $d(k)$, encode the signal into a sum of four single-bit signals, $b_1(k)$, $b_2(k)$, $b_3(k)$, and $b_4(k)$



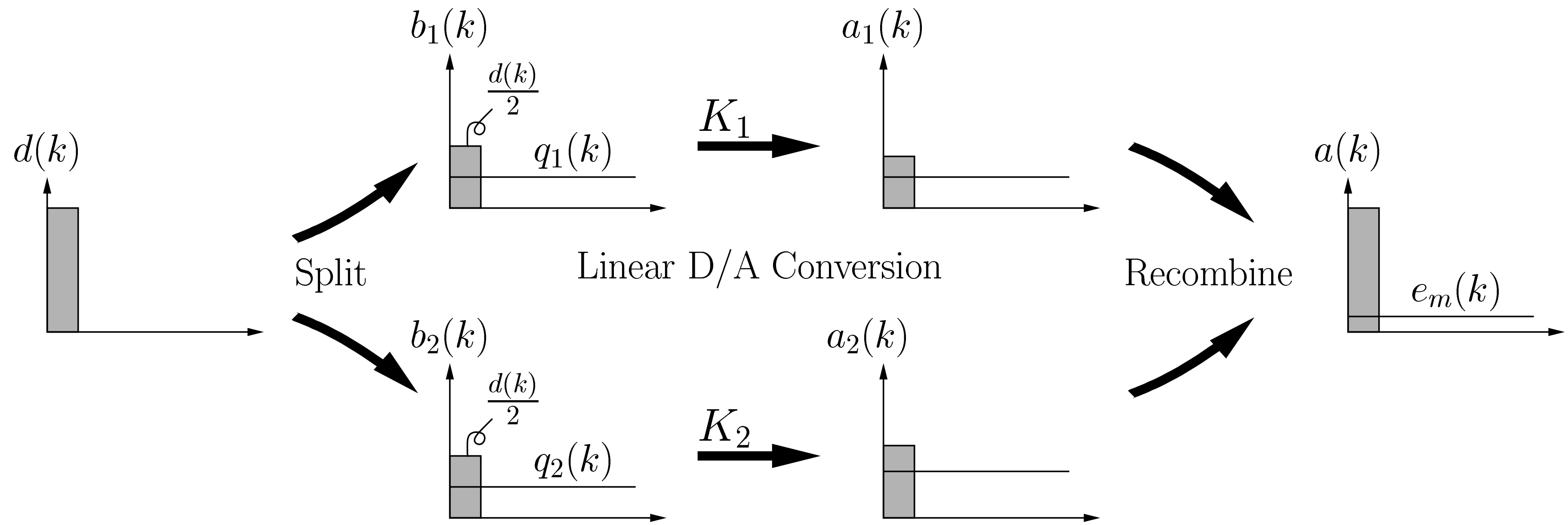
☞ If, e.g., we randomly permute a thermometer-encoded represenation of $d(k)$ and we use all permutations with the same frequency, we may conclude

$$b_i(k) = \frac{d(k)}{4} + q_i(k), \text{where } q_i(k) \text{ are non-auto-correlated random signals}$$

✔ Hence, $e_m(k) = \frac{a(k)}{K_{\mathsf{dac}}} - d(k) = \sum_{i=1}^{4} \frac{\Delta K_{\mathsf{dac},i}}{K_{\mathsf{dac}}} \cdot q_i(k)$ is a random signal with uniform power spectral density

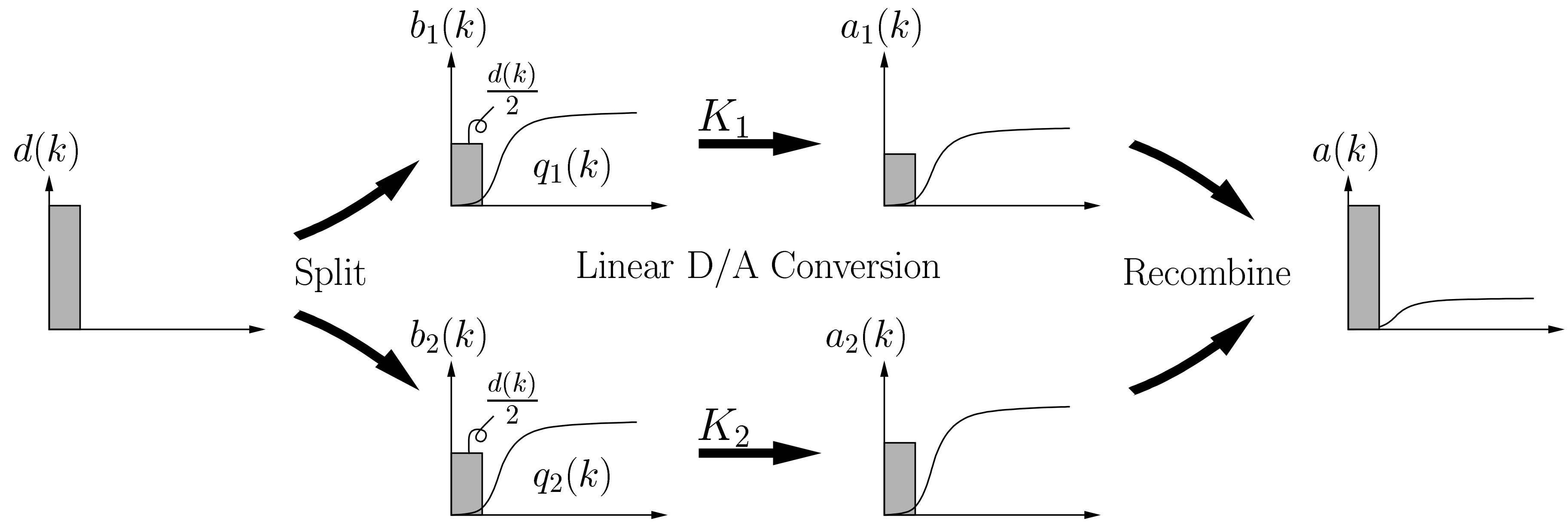
$\boxed{!}$ The power of $e_m(k)$ is signal-dependent; it is maximum for small input signals

How Randomization Circumvents Harmonic Distortion



- ☞ The input signal is decomposed into subsignals: $d(k) = b_1(k) + b_2(k)$
- ☞ The quantization signals cancel each other: $q_1(k) = -q_2(k)$
- ☞ A small DAC gain mismatch is acceptable: $a(k) = \frac{K_1+K_2}{2} \cdot d(k) + (K_1 - K_2) \cdot q_1(k)$
- ☞ The D/A conversions must be linear
  - ✔ This is feasible because the basis signals $b_1(k)$ and $b_2(k)$ are 1-bit signals

The Fundamental Principle in Mismatch-Shaping



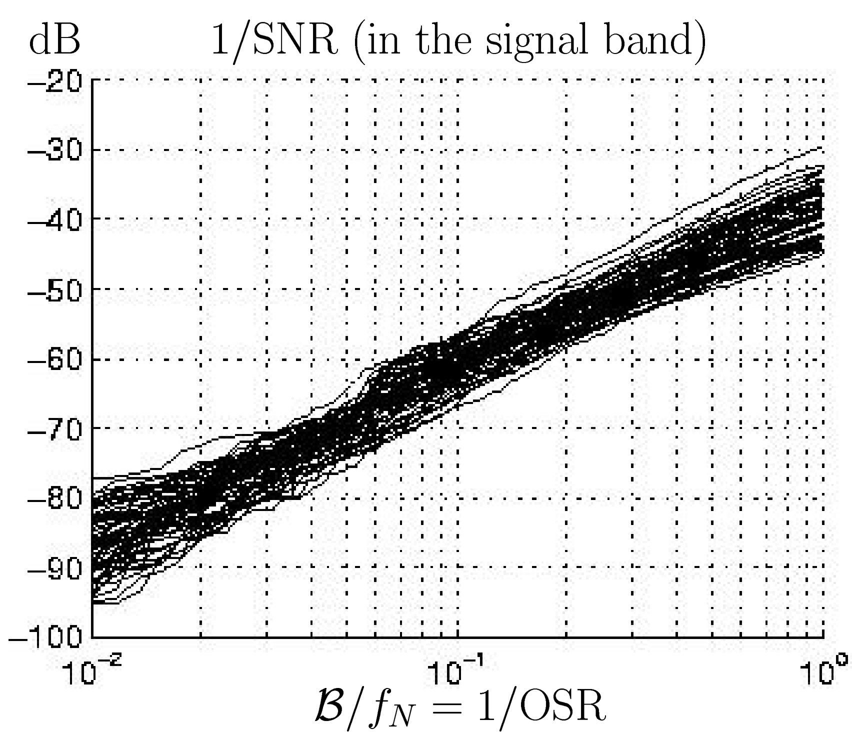
- Mismatch-shaping encoders are generalized $\Delta\Sigma$ modulators: $\sum_i q_i(k) = 0$
- The mismatch-induced error is suppressed by two factors
  - ! Only a relatively small fraction of $q_i(k)$ leaks to the output, say 0.1%
  - ! When properly shaped, only a small fraction of the power in $q_1(k)$ will be in the signal band, say 1%
  - ! The factor by which errors are suppressed is thus: $10^{-3} \cdot 10^{-2} = 10^{-5}$

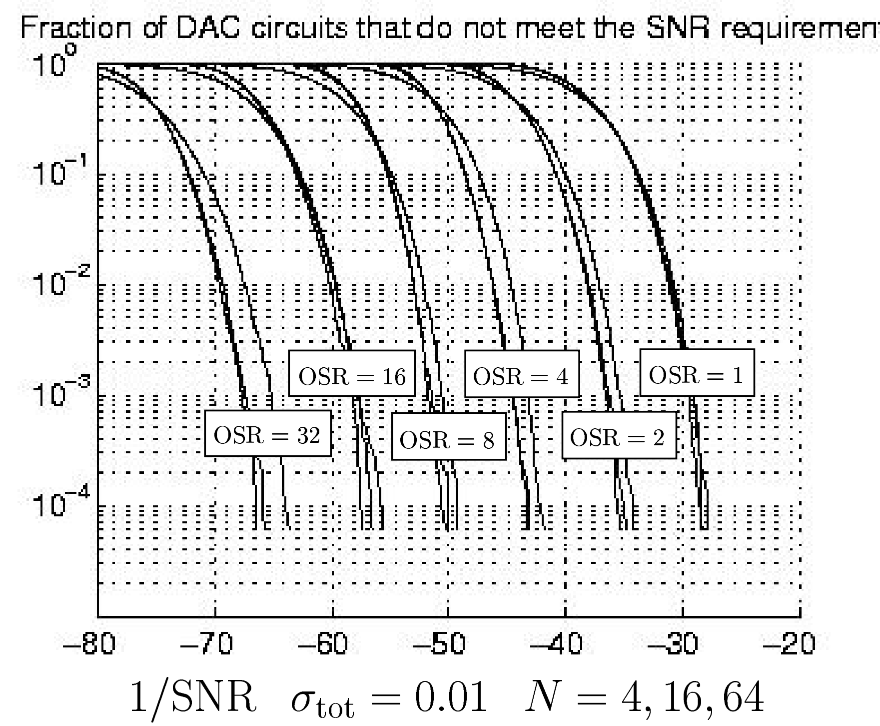
Performance of Mismatch-Shaping DACs

☞ The total power of $e(k)$ is the same as for randomizing DACs

- [!] The resolution (number N of elements) is of little importance
- ✔ The noise is shaped; the SNR increases significantly with the OSR
- [!] 50 dB improvement at OSR $= 100$ (dithered encoder)

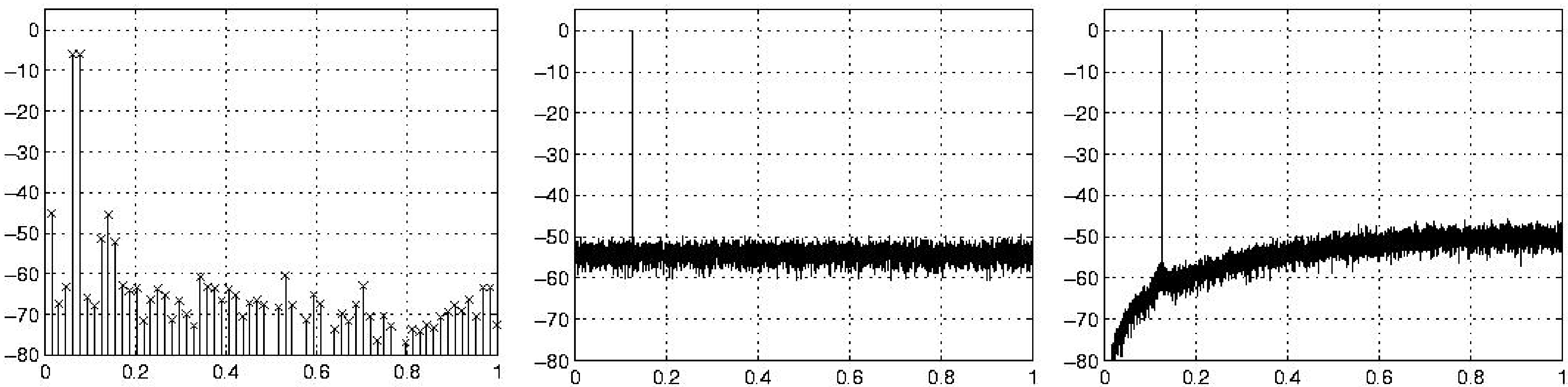
[!] Figures are based on $\sigma_{\text{tot}} = 1\%$ (standard deviation of total DAC capacitance)





Performance Comparison

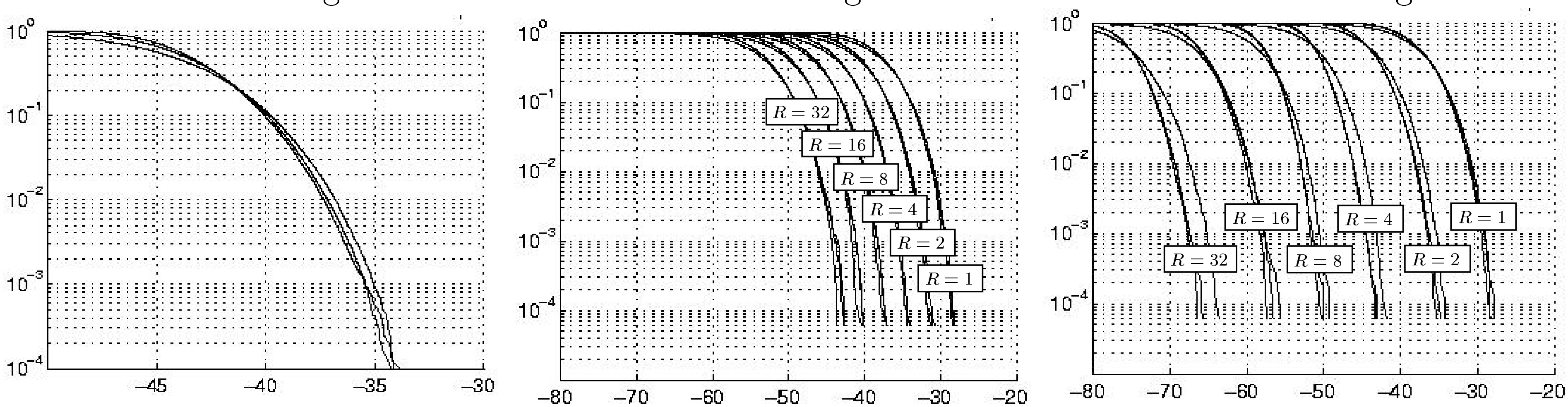
☞ Spectrum and yield resulting from various encoding schemes $\sigma_{\text{tot}} = 1\%$



Thermometer Encoding

Randomizing Encoding

Mismatch-Shaping Encoding



First-Order Mismatch-Shaping is Generally Preferable

- ☞ Second-order algorithms have been developed: $\sum \sum q_i(k)$ bounded
  - ✔ They are characterized by a better suppression of $e(k)$ at low frequencies
  - ✘ However, they barely shape the quantization noise at higher frequencies
  - ✘ They are also characterized by a higher circuit complexity
- ☞ First-order algorithms are preferable for OSR ≤ 25
  - ✔ Up to 30 dB $(20$ dB$)$ suppression may be obtained at OSR $= 10$
  - ✘ Beware of idle tones!